REMARKS/ARGUMENTS

After entry of this amendment, claims 1-2, 5-8, 11-13, and 18-21 will be pending in this application.

Claims 1-2, 7-8, 13, and 18-19 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gray et al., United States patent number 6,816,923, in view of Abramson et al., United States patent number 6,499,077, Iizuka et al., United States patent number 5,581,530, and Nguyen et al., United States patent number 5,355,326. Claims 5, 11, and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gray in view of Abramson, Iizuka, Nguyen and Kuronuma et al., United States patent number 6,859,848. Claims 6, 12, and 21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gray in view of Abramson, Iizuka, Nguyen and "Microsoft Computer Dictionary."

Reconsideration of these rejections and allowance of the pending claims in light of these amendments and remarks is respectfully requested.

Claim 1

Claim 1 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gray in view of Abramson, Iizuka, and Nguyen. But this combination of cited references does not show or suggest each and every element of this claim. For example, claim 1 recites "a plurality of buffers in the memory interface, each of the plurality of buffers sized to store a data burst for a memory access request." The combination of cited references does not show or suggest this feature in combination with the other recited limitations.

The pending office action cites several passages in Iizuka as showing or suggesting this feature. (See pending office action, page 10, fourth paragraph.)

In these passages, Iizuka shows the operation of buffers in an audio device during record and play modes. (See Iizuka, column 11, lines 5-20.) Iizuka further shows that each buffer is sized to hold a number of samples. Iizuka does not show that a number of samples corresponds to a data burst for a memory access request. Thus, Iizuka does not show that each of the plurality of buffers is sized to store a data burst for a memory access request.

The pending office action appears to recognize that Iizuka does not show this feature, and instead cites Gray as showing storing a data burst from memory. (See pending office action, page 2, last paragraph.) The rejection is thus understood to be that since Gray stores data bursts and Iizuka shows buffers sized to hold a number of samples, the combination results in buffers sized to hold data bursts.

However, the pending office action does not provide motivation for why it would be obvious to combine these references. Moreover, there is no motivation provided in either Gray or Iizuka as to why either would use buffers sized to store data bursts. The only motivation for this combination appears to be impermissible hindsight.

The pending office action recognizes that Abramson does not show or suggest this feature. (See pending office action, page 10, second paragraph.) Nguyen adds nothing to this. Accordingly, the combination of cited references does not show or suggest a plurality of buffers in the memory interface, each of the plurality of buffers sized to store a data burst for a memory access request, as is required by the claim.

Claim 1 further recites "wherein, for a wrapping memory access request requiring multiple buffers, data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer by the control logic." The combination of cited references does not show or suggest this feature.

The pending office action cites Figure 8 of Iizuka as showing or suggesting this feature. (See pending office action, page 8, last paragraph.)

In Figure 8, Iizuka shows three buffers, 9-1 to 9-3. (See Iizuka, Figure 8.) Each buffer stores a sample. (See Iizuka, column 11, lines 20-25.) Each buffer is a FIFO operating as a ring buffer. (*id.*) In this configuration, a start and end address for each sample are stored in a buffer 9-1 to 9-3. Data in buffers 9-1 to 9-3 are transferred to a hard drive using DMA transfers. (See Iizuka, Figure 8.)

Thus, Iizuka does not show a wrapping memory access request. Instead, Iizuka shows that each sample is stored in a single buffer. Iizuka does not show that a sample needs to be wrapped using multiple buffers. Because of this, Iizuka does not show that data required for a

beginning and end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer. Instead, Iizuka shows that the beginning and end of each sample is stored in its own buffer 9-1 to 9-3.

The pending office action appears to recognize that Iizuka does not show this feature, and instead appears to indicate that Iizuka in combination with one or more other references shows this feature. (See pending office action, page 3, last paragraph.) However, this is not further elaborated upon, and no motivation for any such combination is given.

The pending office action recognizes that Gray and Abramson do not show or suggest this feature. (See pending office action, page 10, second paragraph.) Nguyen adds nothing to this. Accordingly, the combination of cited references does not show or suggest wherein, for a wrapping memory access request requiring multiple buffers, data required for each of a beginning and an end of the wrapping memory access request are assigned to respective sub-buffers of a single respective buffer by the control logic, as is required by the claim.

Claim 1 further recites "wherein the control logic records a value of a pointer indicating a first sub-buffer of the single respective buffer storing the end data, such that the control logic is able to return to the indicated first sub-buffer to retrieve the end data from the single respective buffer." The combination of cited references does not show or suggest this feature.

The pending office action cites Nguyen as showing or suggesting this feature. (See pending office action, page 9, last paragraph.)

Nguyen shows the use of input and output pointers. (See Nguyen, Figure 2.) The input pointer points to the next slot involved in an input operation, while the output pointer points to the next slot involved in an output operation. (See Nguyen, column 6, lines 4-7.) Nguyen does not show that these pointers allow control logic to return to the indicated first sub-buffer to retrieve the end data from the single respective buffer. Instead, Nguyen shows an input pointer that points to a next slot involved in an input operation and an output pointer that points to the next slot involved in an output operation.

The pending office action appears to recognize that Nguyen does not show this feature, and instead states that the previous office action "relied mainly on Iizuka for the teaching" of this feature. (See pending office action, page 4, second paragraph.) The pending office action further cites several passages in Iizuka. However, as described above, Iizuka does not show memory wrapping, and thus cannot show a pointer that allows control logic to return to the indicated first sub-buffer to retrieve the end data from the single respective buffer. Moreover, no motivation for combining Iizuka and Nguyen in a manner to show this feature is given.

The pending office action recognizes that Gray and Abramson do not show or suggest this feature. (See pending office action, page 12, first full paragraph.) Accordingly, the combination of cited references does not show or suggest wherein the control logic records a value of a pointer indicating a first sub-buffer of the single respective buffer storing the end data, such that the control logic is able to return to the indicated first sub-buffer to retrieve the end data from the single respective buffer, as is required by the claim.

For at least these reasons, claim 1 should be allowed.

Other claims

Claims 7, 13, and 18 should be allowed for similar reasons as claim 1. The remaining rejected claims depend on one of the above claims and should be allowed for at least the same reasons and the additional limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

/ *J. Matthew Zigmant* /

J. Matthew Zigmant
Reg. No. 44,005

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
JMZ:deb
62179859 v1